WHAT IS CLAIMED IS:

1. A method of tuning a voltage controlled oscillator comprising:

measuring a frequency of oscillation of the voltage controlled oscillator;

comparing the frequency of oscillation to a desired frequency;

generating a logic signal; and

applying the logic signal to a resistor,

wherein the resistor is coupled to a first capacitor and a second capacitor, the first capacitor is coupled to an inductor, and the second capacitor is coupled to a first supply terminal.

2. The method of claim 2 wherein the second capacitor is a junction varactor.

3. The method of claim 2 wherein the second capacitor is a MOS varactor.

4. The method of claim 2 wherein the first supply terminal is ground.

5. An integrated circuit having a voltage controlled oscillator comprising:

a first inductor;

a first capacitor coupled to the first inductor;

a first varactor diode coupled to the first capacitor; and

a first isolation resistor coupled to the first capacitor and the first varactor diode,

wherein the first isolation resistor is configured to receive a control voltage.

6. The integrated circuit of claim 5 further comprising:

a second inductor;

a second capacitor coupled to the first inductor;

a second varactor diode coupled to the first capacitor;

a second isolation resistor coupled to the second capacitor and the second varactor diode, wherein the second isolation resistor is configured to receive the control voltage;

a first device having a drain coupled to the first inductor and a gate coupled to the second inductor; and

a second device having a drain coupled to the second inductor and a gate coupled to the first inductor.

7. The integrated circuit of claim 6 further comprising:

a current source coupled to a source of the first device and a source of the second device.

8. The integrated circuit of claim 7 wherein the current source is a common source device.

9. The integrated circuit of claim 7 wherein the first device and the second device and n-channel CMOS devices.

10. An integrated circuit having a voltage controlled oscillator comprising:

a first inductor;

a second inductor;

a first capacitor coupled to the first inductor;

a second capacitor coupled to the first inductor;

a third capacitor coupled to the first capacitor;

a fourth capacitor coupled to the second capacitor;

a first isolation resistor coupled to the first capacitor and the third capacitor, wherein the first isolation resistor is configured to receive a control voltage;

a second isolation resistor coupled to the second capacitor and the fourth capacitor, wherein the second isolation resistor is configured to receive the control voltage;

a first device having a drain coupled to the first inductor and a gate coupled to the second inductor; and

a second device having a drain coupled to the second inductor and a gate coupled to the first inductor.

11. The integrated circuit of claim 10 further comprising:

a current source coupled to a source of the first device and a source of the second device.

12. The integrated circuit of claim 11 wherein the current source is a common source device.

13. The integrated circuit of claim 11 wherein the first device and the second device and n-channel CMOS devices.

14. The integrated circuit of claim 11 wherein the third and fourth capacitors are junction varactors.

15. The integrated circuit of claim 11 wherein the third and fourth capacitors are MOS varactors.

16. The integrated circuit of claim 11 wherein the control voltage is a logic signal.

17. The integrated circuit of claim 11 wherein the control voltage is an analog signal.

18. The integrated circuit of claim 10 wherein the integrated circuit is an RF transceiver.

19. A phase-locked loop comprising:

a phase detector configured to receive a reference clock;

a low-pass filter coupled to the phase detector;

a voltage-controlled oscillator coupled to the low-pass filter; and

a divider coupled between the voltage-controlled oscillator and the low-pass filter,

wherein the voltage-controlled oscillator comprises:

a first inductor;

a second inductor;

a first capacitor coupled to the first inductor;

a second capacitor coupled to the first inductor;

a third capacitor coupled to the first capacitor;

a fourth capacitor coupled to the second capacitor;

a first isolation resistor coupled to the first capacitor and the third capacitor, wherein the first isolation resistor is configured to receive a control voltage;

a second isolation resistor coupled to the second capacitor and the fourth capacitor, wherein the second isolation resistor is configured to receive the control voltage;

a first device having a drain coupled to the first inductor and a gate coupled to the second inductor; and

a second device having a drain coupled to the second inductor and a gate coupled to the first inductor.

20. The integrated circuit of claim 19 wherein the first device and the second device and n-channel CMOS devices.

21. The integrated circuit of claim 19 wherein the third and fourth capacitors are junction varactors.

22. The integrated circuit of claim 19 wherein the third and fourth capacitors are MOS varactors.

23. An electronic system comprising the phase-locked loop of claim 19.